REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-7 and 19-31 are presently active in this application, Claims 1, 7, 21 and 27 having been amended, Claims 8-18 canceled, and new Claims 30 and 31 added by the present amendment.

In the outstanding Office Action, Claims 8-18 were withdrawn from consideration, Claims 1-7, 19 and 20 were rejected under 35 U.S.C. §102(b) as being anticipated by Kim et al. (U.S. 5,182,224, hereinafter called "Kim"), and Claims 21-29 were rejected under 35 U.S.C. §102(b) as being anticipated by Tadaki et al. (U.S. 5,349,218, hereinafter called "Tadaki").

In view of the new grounds for rejection, Claims 1, 7, 21 and 27 have been amended to clarify the claimed invention, and Claims 30-31 have been added to vary the claim scope recited in the pending claims. The feature added to Claims 1 and 21 is supported by FIGS. 1A and 10A and the description in the specification, at page 16, lines 20-25. Claims 7 and 27 are amended for consistency with the recitation of features stated in Claims 1 and 21. New Claims 30 and 31 are supported by FIG. 1A, etc. No new matter has been added.

Briefly recapitulating, amended Claims 1 and 21 recite a semiconductor memory device including, inter alia, a first insulation layer which is formed on the inner surface of a trench and has the top located above the surface of a semiconductor substrate, and a device isolation insulation layer which has in its surface a concave whose bottom is located below the top of a first conductive layer.

As described in the specification, page 16, lines 11-25, when portions of a top insulation layer 16 on a storage node electrode 13 are removed to expose the top of the

storage node electrode 13, the conditions of overetching is employed for ensuring exposure of the storage node electrode 13. At the same time, a device isolation insulation layer 17 whose surface is not covered is partly etched to the extent of a position lower than the top of the storage node electrode 13.

Kim in FIG. 1 shows a structure including a general trench-type capacitor. However, the top of an oxide film 16 formed on the inner surface of a trench 21 is not located above the surface of a substrate 1.

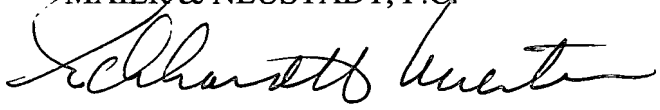
It appears that the outstanding rejection is based on the finding that the bottom of the Kim insulating oxide film layer 9 is equivalent to the surface of the substrate 1. In that case, it should be recognized that the top of the oxide film 16 is located above the surface of the substrate 1 in accordance with the description that the top of the oxide film 16 is located above the bottom of the insulating oxide film layer 9. However, the Kim insulating oxide film layer 9 is formed by the technique of local oxidation of silicon, not a substrate. In the Kim device, the surface of the substrate 1 is located, for example, at the boundary between an N+ diffusion region 11 and a POLY layer 7, and at the same level as the top of the oxide film 16. It is therefore respectfully submitted that Kim fails to disclose or obviate the structure recited in amended Claims 1 and 21, and that the outstanding rejection based on Kim has been overcome.

Turning now to the Tadaki reference, Tadaki in FIG. 2 discloses the top of a dielectric film 32 is located above the surface of a substrate 21. However, an element isolating insulating film 24 of Tadaki does not include any concave whose bottom is located below the top of a poly-silicon layer 33. In view of this deficiency, it is respectfully submitted that

Tadaki fails to disclose or obviate the structure recited in amended Claims 1 and 21, and that the outstanding rejection based on Tadaki also has been overcome.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

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